What is Claimed:

1. A variable condition responsive sensor system comprising at least one variable condition sense element having first and second outputs, the variable condition being one of pressure, acceleration, force and torque,

first and second signal conditioning paths, the first output of the at least one sense element connected to the first signal conditioning path and the second output of the at least one sense element connected to the second signal conditioning path,

memory for storing calibration and characterization data for the at least one sense element and the signal conditioning paths, and

an interface circuit for transmitting data from the memory to the signal conditioning components for separately conditioning the signals of the at least one sense element and to an external controller to perform mathematical corrections of the conditioned signals and for comparing the conditioned signals of the at least one sense element.

2. A variable condition responsive sensor according to claim 1 in which the at least one variable condition sense element comprises first and second half bridges, the first half bridge providing the first output and the second half bridge providing the second output.

3. A variable condition responsive sensor system according to claim 2 in which there are a plurality of sense elements and further comprising at least one multiplexer with addressable ports connected to the outputs of each half bridge of the plurality of sense elements, the at least one multiplexer having output ports, an output port connected to each signal conditioning path.

4. A variable condition responsive sensor system according to claim 2 in which each half bridge has a bias node and a ground node and further

comprising an independent variable resistor connected in series between a voltage source and an output port of the at least one multiplexer.

5. A variable condition responsive sensor system according to claim 3 in which the signal conditioning paths and the at least one multiplexer are formed in an ASIC.

6. A variable condition responsive sensor system according to claim 5 in which the memory is non-volatile.

7. A variable condition responsive sensor system according to claim 6 in which the non-volatile memory is formed in a separate IC.

8. A variable condition responsive sensor system according to claim 1 in which the variable condition is pressure.

9. A variable condition responsive sense element system comprising

a plurality of variable condition responsive sense elements providing an output dependent on the variable condition, the variable condition being one of pressure, acceleration, force and torque, the sense elements each having first and second half bridges, each bridge half having a bias node, a ground node and a respective positive and minus output node,

a voltage source,

an electronic circuit having first, second , third and fourth multiplexers, each having an output and a plurality of address input positions,

a respective independent variable resistor connected in series between the voltage source and the output of each of the first and third multiplexers, the bias node of each half bridge of each sense element connected to a respective multiplexer address position of the respective first and third multiplexers,

separate signal conditioning paths,

the minus output node of each sense element connected to a respective multiplexer address position of the second multiplexer, the positive node of each sense element connected to a respective multiplexer address position of the fourth multiplexer,

a respective separate signal path connected to the output of each multiplexer,

an analog to digital converter having a plurality of inputs and an output, the signal paths being connected to the inputs of the analog to digital converter,

a data register having an input and an output, the output of the analog to digital converter connected to the input of the data register,

a data transfer circuit connected to the data register and having connections for an external controller, and

data transmitted to and received from the external controller through the data transfer circuit, a memory, the memory section being connected to the data transfer circuit, the memory providing analog trim settings for the sense element signal paths, and data for the external controller enabling the external controller to perform mathematical compensation for the variable condition sense element signals.

10. A variable condition responsive sensor system according to claim 9 in which the data transfer circuit is a serial peripheral interface bus.

11. A variable condition responsive sensor system having a plurality of variable condition sense elements, the method of

forming each of the sense bridge elements into two portions, each portion having an output node,

separately conditioning output signals from each output node of a selected sense element,

comparing the separately conditioned signals of the portions of the selected sense element with each other to determine whether the conditioned signals come within selected tolerance bands.

12. The method claim 11 in which the variable condition sense elements each comprise a bridge having two halves, each half having one of the output nodes.

13. The method of claim 12 in which the step of comparing the separately conditioned signals includes subtracting the conditioned signal of one half bridge from the conditional signal of the other half bridge of a sense element and taking the average of the difference in the two conditioned signals.

14. The method of claim 12 further comprising

forming an electronic circuit having signal conditioning paths, the paths having signal conditioning components for each half bridge output,

obtaining electronic calibration data for each sense element during manufacture of the sensor system and storing that information in memory,

connecting the outputs of the bridge halves of a selected sense element to the respective signal conditioning circuit paths using basic calibration data from the memory and separately, partially conditioning the selected output signal, and

completing the separate conditioning of the partially conditioned signal by performing mathematical corrections using data transferred from the non-volatile memory to obtain fully conditioned signals before the comparison step of the separately conditioned signals.

15. The method of claim 12 further comprising

forming an electronic circuit having multiplexers, a signal conditioning path having signal conditioning components for each half bridge output, an

analog to digital converter, memory and an interface circuit for transmitting and receiving data,

obtaining electronic calibration data for each half bridge sense element during manufacture of the sensor system and storing that information in memory,

connecting the electronic circuit to an external controller,

transmitting data from memory to enable the external controller to perform mathematical corrections to a conditional digital signal,

selecting an address of the multiplexers for connecting the output of a selected half bridge of a selected sense element to the respective signal conditioning circuit path and to transmit basic calibration data to the signal conditioning components in the signal conditioning path,

partially conditioning the addressed sense element half bridge using the basic calibration data transmitted from memory to provide a partially conditioned signal,

converting the partially conditioned signal from an analog format to a digital format in the analog to digital converter to provide a digital signal,

transmitting the digital signal to the external controller,

completing the conditioning of the partially conditioned signal by performing mathematical corrections to the digital signal in the external controller using the data transferred from the memory to obtain fully separately conditioned signals before the comparison step of the separately conditioned signals.

16. The method of claim 15 in which the interface circuit comprises a serial peripheral interface bus.

17. The method of claim 15 in which each half bridge has a bias node and further comprising the step of multiplexing the bias node into connection with an independent variable resistor serially connected to a voltage source.